In the Claims

34. [Original] A computer system comprising:

a memory controller;

a common display memory and main memory comprising at least one internal memory subsystem contained in the memory controller and at least one external memory subsystem outside of the memory controller;

at least one multi-use memory channel operatively coupled to the at least one internal memory subsystem and the at least one external memory subsystem;

a memory channel data switch coupled to the memory controller and configured to dynamically allocate the at least one multi-use memory channel; and

a central processing unit (CPU) subsystem controller operably coupled to the memory channel data switch and the memory controller, the CPU configured to output control signals to the memory channel data switch and the memory controller.

35. [Original] The computer system of claim 34 further comprising a multiplexer configured to selectively couple at least one external memory subsystem to one of the at least one multi-use memory channels.

36. [Original] The computer system of claim 34 wherein one of the at least one internal memory subsystem and the at least one external memory subsystem is a display memory subsystem configured to be able to function as main system memory.

5.

37. [Original] The computer system of claim 34 wherein at least one of the at least one internal memory subsystem and the at least one external memory subsystem includes a data manipulator containing a plurality of data storage elements.

6.

38. [Original] The computer system of claim 34 further comprising a complete drawing buffer configured to permit a graphics engine to store display output data and transfer the display output data for subsequent display updates.

7.

B1 cnt

39. [Original] The computer system of claim 34 further comprising a computer display, a complete drawing buffer and a graphics engine, wherein the graphics engine is configured to be able to store output data in the drawing buffer for output to the computer display and to subsequently transfer the output data to the computer display for display updates.

8.

40. [Original] A computer system comprising:

a display;

a memory controller;

common display memory and main memory comprising at least one of an internal memory subsystem included within the memory controller and configured to cooperatively couple therewith, and at least one of an external memory subsystem outside of the memory controller and configured to cooperatively couple therewith;

B

a plurality of memory channels operatively coupled to the common display memory and main memory, at least one of the plurality of memory channels configured as a multi-use memory channel;

a memory channel data switch operably coupled to the memory controller and to the plurality of memory channels and configured to allocate selected ones of the plurality of memory channels between the at least one internal memory subsystem and the at least one external memory subsystem;

a central processing unit (CPU) subsystem controller operably coupled to the memory channel data switch and the memory controller and configured to produce output signals to be applied to the memory channel data switch and memory controller;

B1 Cont

a graphics/drawing and display subsystem operably coupled to the CPU subsystem controller, the memory channel data switch and the memory controller, the graphics/drawing and display subsystem being configured to provide output signals to the memory channel data switch and the memory controller;

an arbitration and control engine operably coupled to the CPU subsystem controller, the graphics/drawing and display subsystem, the arbitration and control engine being configured to provide output signals to the CPU subsystem controller and to the graphics/drawing and display subsystem; and

a peripheral bus controller operably coupled to the memory channel data switch, the memory controller and the arbitration and control engine and configured to provide output signals to the memory channel data switch, the memory controller and the arbitration and control engine.

B

9.
~~41.~~ 8 [Original] The computer system of claim ~~40~~ wherein at least one of the at least one internal memory subsystem and the at least one external memory subsystem includes DRAM memory.

11.
~~10.~~
~~42.~~ 8 [Original] The computer system of claim ~~40~~ wherein at least one of the at least one internal memory subsystem and the at least one external memory subsystem comprises a data manipulator containing a plurality of storage elements.

12
~~11.~~
~~43.~~ 8 [Original] The computer system of claim ~~40~~ further comprising a computer display, a complete drawing buffer and a graphics engine, wherein the graphics engine can store output data in the drawing buffer for output to the computer display and subsequently transfer the output data to the computer display for display updates.

B7 CONT

3.
~~12.~~
~~44.~~ 2 [New] The computer system of claim ~~36~~ wherein one of the at least one internal memory subsystem and the at least one external memory subsystem is a display memory subsystem configured to be able to function as main system memory.

10.
~~13.~~
~~45.~~ 9 [New] The computer system of claim ~~41~~ wherein at least one of the at least one internal memory subsystem and the at least one external memory subsystem comprises a data manipulator containing a plurality of storage elements.

B